Philips, STMicroelectronics, TSMC

An R&D alliance for leadership in CMOS process technology

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Reasons for semiconductor companies to co-operate

- ITRS roadmap acceleration:
  a new generation every two years
- Increasing complexity
  - Core process
  - Options
- Increasing R&D costs
  - Sharing costs by co-operation
- Core process design rules standardization
  - Attracting IP providers

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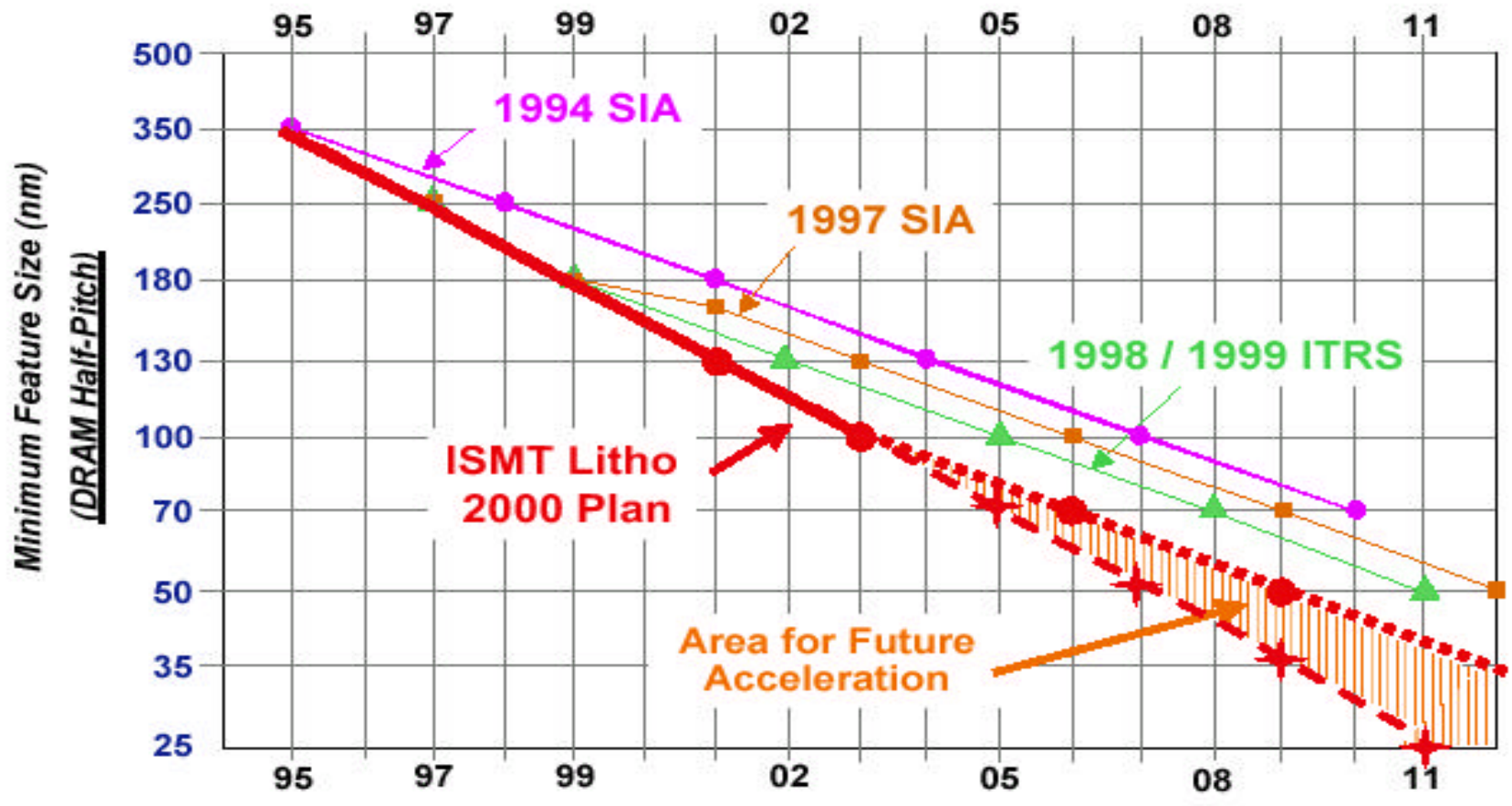
ITRS Roadmap Potential Acceleration



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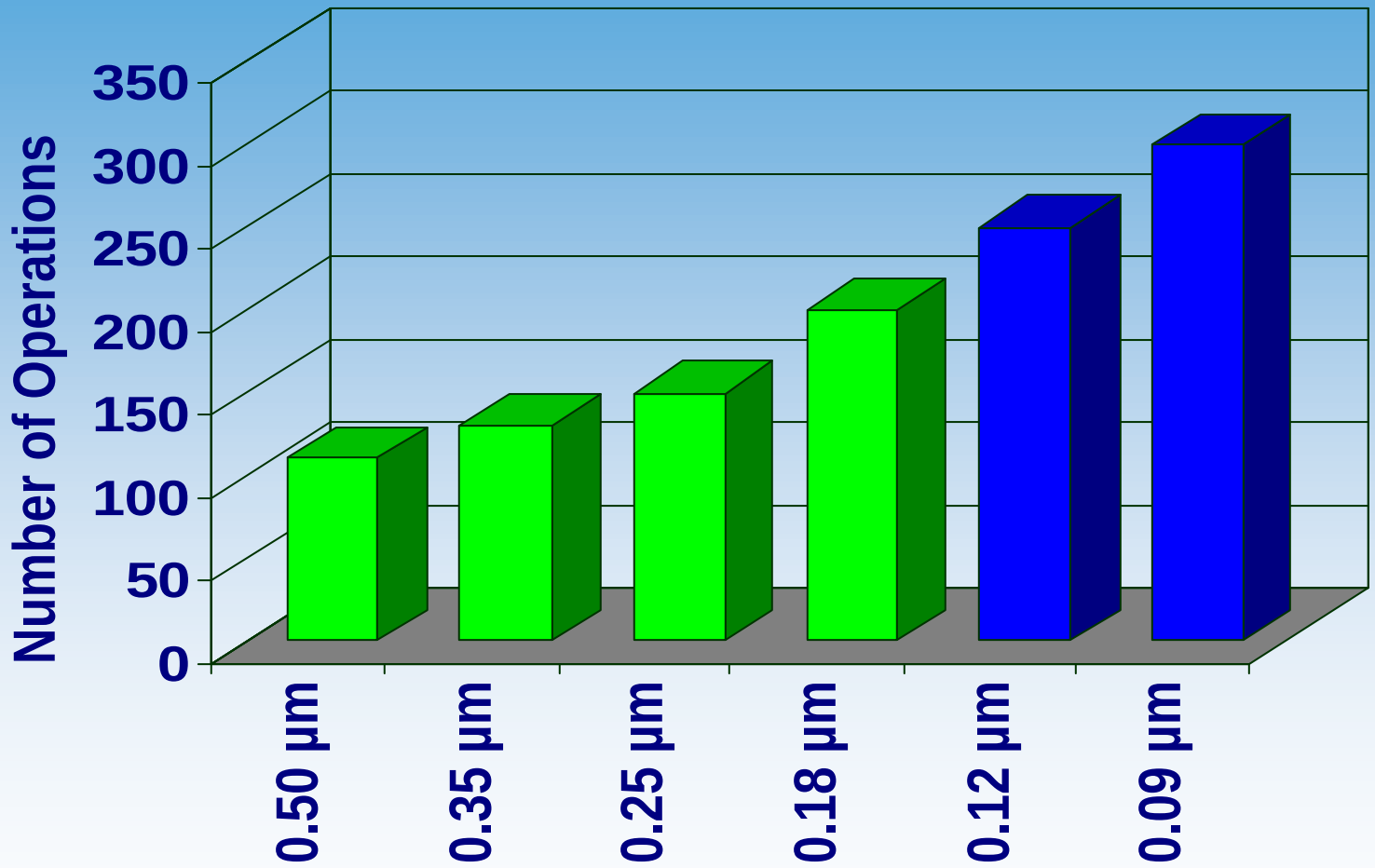
CMOS Core Process Complexity Increase



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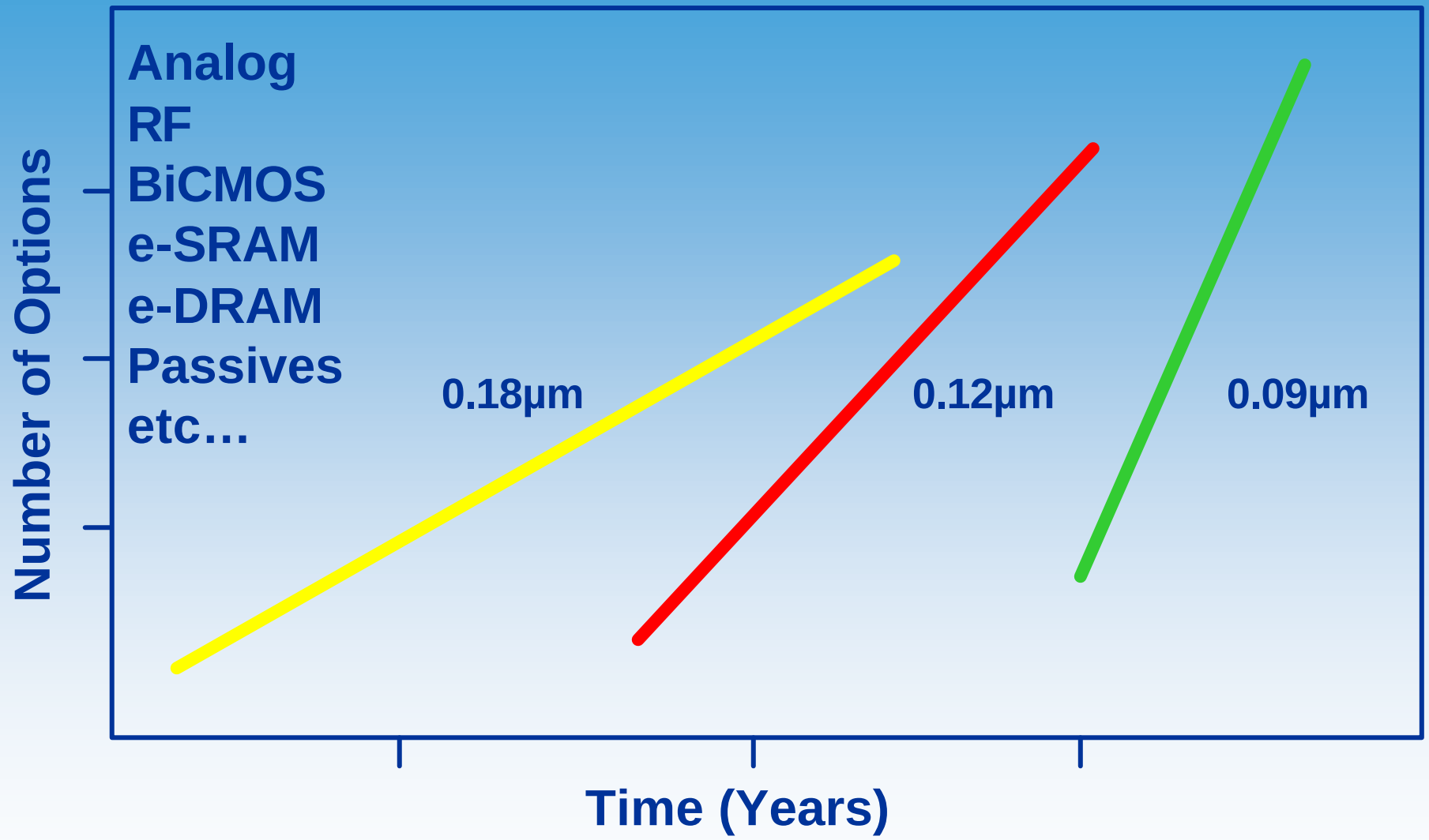
More options in less time



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Philips, ST and TSMC co-operation enables each company:

- To offer customers easy access to third-party IP based on a well-accepted standard
- To offer fast access to volume capacity and compatible second sourcing from the beginning
- To reinforce their worldwide standard
- To develop and easily implement options for '**System-on-Chip**'

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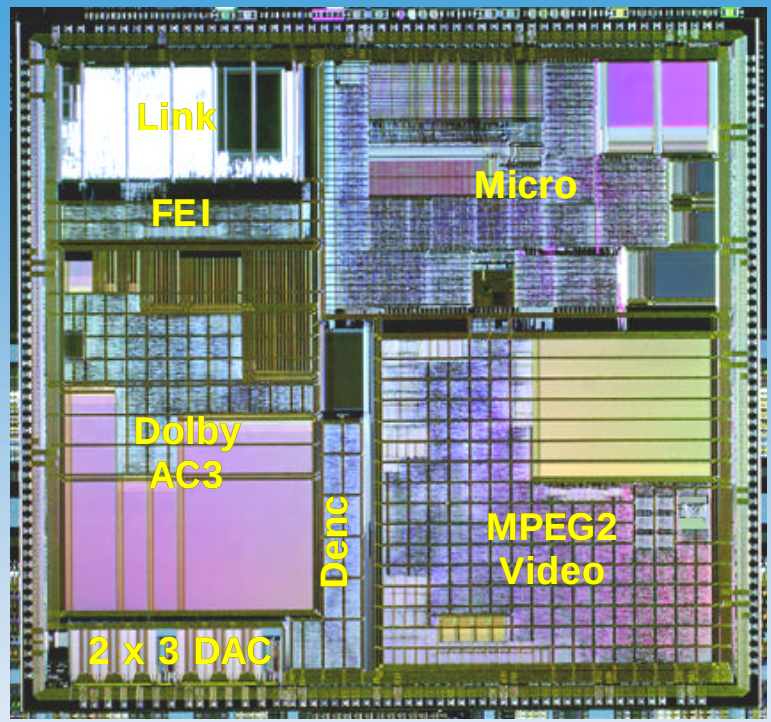
System-on-Chip Challenges

Time-to-market

Time-to-volume

Process roadmap acceleration

Consumerization of electronic devices



Complex systems

µCs, DSPs HW/SW

SW protocol stacks

RTOS

Digital/Analog IP

On-Chip busses

Deep sub-micron effects

crosstalk

electro migration

wire delay

mask cost (OPC, PSM)

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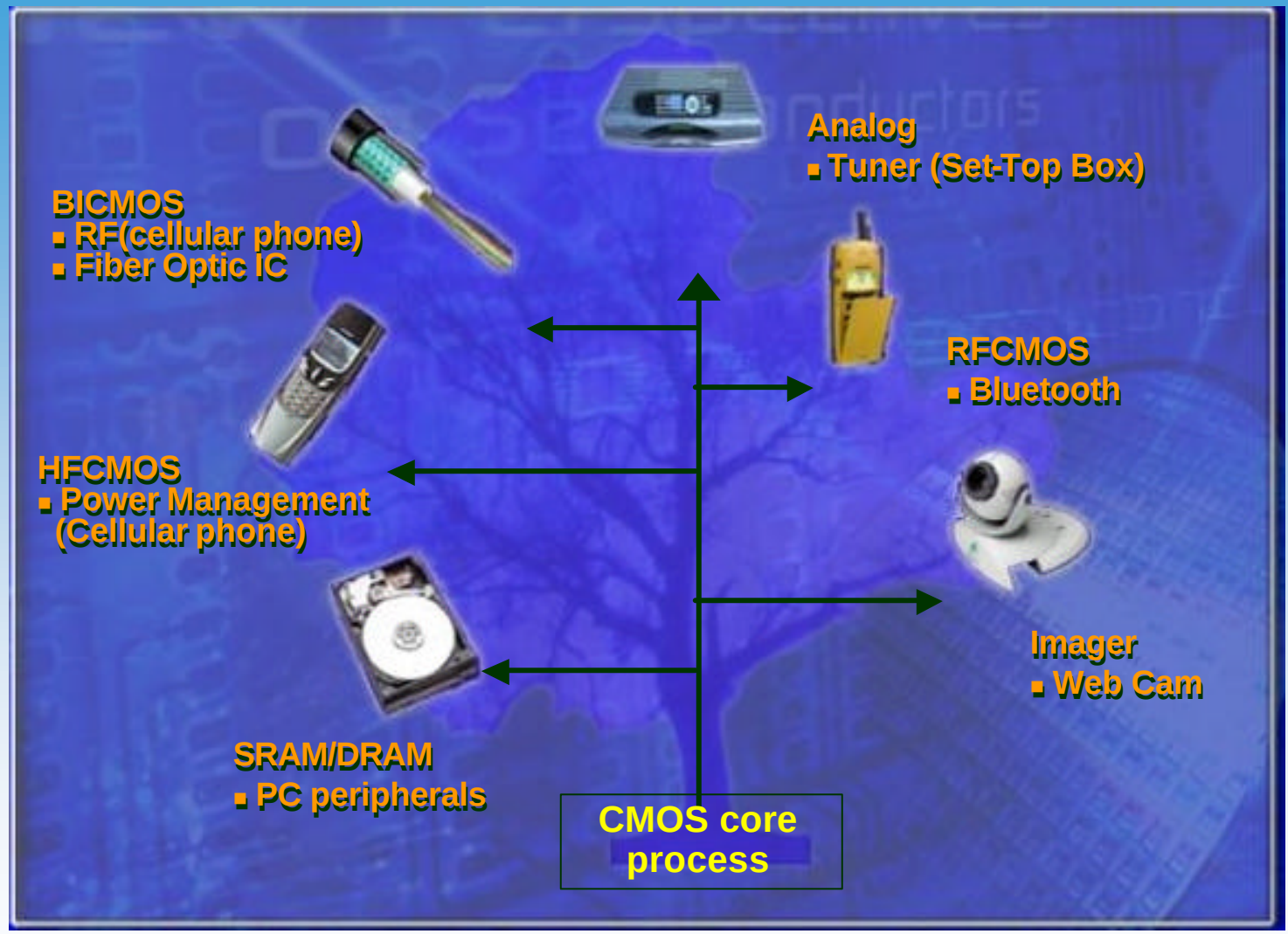
CMOS Options for System-on-Chip



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System-on-Chip Approach

Concurrent Engineering

Early access for customers to prototyping and volume

Co-operation Benefits

- Process & options development
- Pilot line and volume production
- UNICAD tools & methods
- Cores & IP: µP, DSP, RAM, ROM,...
- HW - SW codesign
- HW emulation

Technology Platform

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ST and Philips - Long term partners

- ST and Philips have been partners in CMOS process development since 1992; longest ongoing partnership in the industry
- Successfully developed technology nodes of 0.5µ, 0.35µ, 0.25µ, 0.18µ (all in production) and 0.12µ (pilot production)
- Since 01-01-2001 in Crolles2: 300mm R&D and pilot fab
- Jointly developing 0.09µ (90 nm) process, libraries and IP
- Aggressive scheme bringing leadership in technology

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TSMC and Philips - Long term partners

- Philips co-founder of TSMC; still minority shareholder
- Long term foundry relationship
- R&D co-operation from the start

The JDP links these partners around a common goal:

Developing leading CMOS technology for the
90 nm and smaller geometry nodes
creating a de facto industry standard

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Essence of the JDP

- Joint development project that focuses on R&D for production of advanced CMOS processes at 90 nm, 65 nm and beyond
- Philips, ST and TSMC co-define the process architecture and parameters
- Both develop, in own R&D center, processes and core libraries and exchange the know-how
- Processes are fully compatible (design rule and electrical)
- Test and characterization runs in both fabs (Crolles2 and Hsin-Chu) to show compatibility and accelerate yield improvement
- Exchange of engineers between Crolles2 and Hsin-Chu
- Exchange of best practices

JDP phasing

- 5 year program, started mid 2001
- Has started with 90 nm
- Soon followed with 65 nm process
- Support by research partners (Philips Research / IMEC and LETI, France Telecom R&D)

- Initial development of general purpose process
- Subsequently low-power and high-performance options
- Includes value added options
  - embedded memory (SRAM, DRAM)
  - analog

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Advantages (1)

For the partners

- Combine the creative resources to define the most advanced process
- Input from large customer base
- Share efforts in library and IP generation
- Accelerated learning (a/o yield)
- Provides a means to become a leader in SoC design

Advantages (2)

For our customers

- Faster access to state-of-the-art processes with piloting facilities
- Immediate and automatic multiple sourcing (risk reduction)
- Rich library and potentially large availability of IP

For the industry

- De facto process standard encourages IP generation and exchange
- Tool vendors get an extended user base

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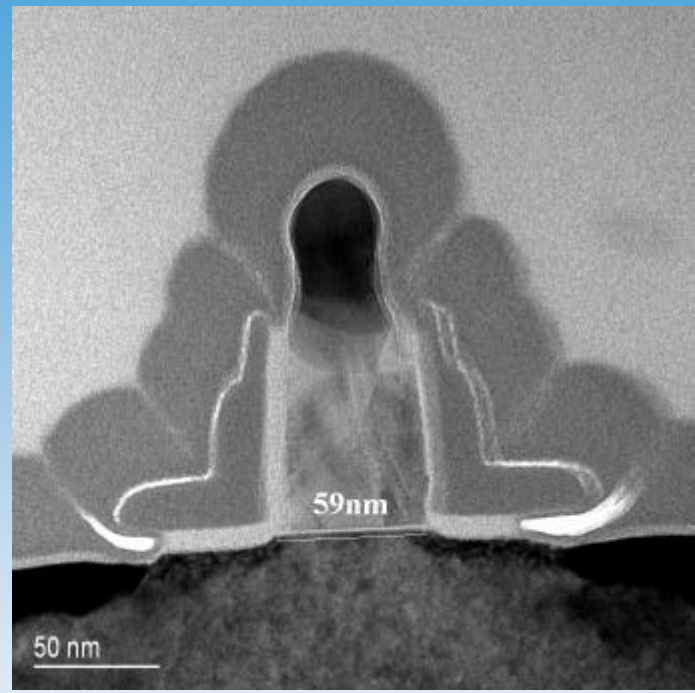
Industry-first 90 nm CMOS logic

- Early availability of 90 nm logic technology
- Highly competitive price / performance
- Optimized general purpose, low power and high speed versions
- Special attention given to SoC options
  - High gate density
  - Embedded memories



Cross-section of high-speed 90 nm transistor

Node	90 nm	120 nm	180 nm
Density *Kgates/mm²*	362	197	92

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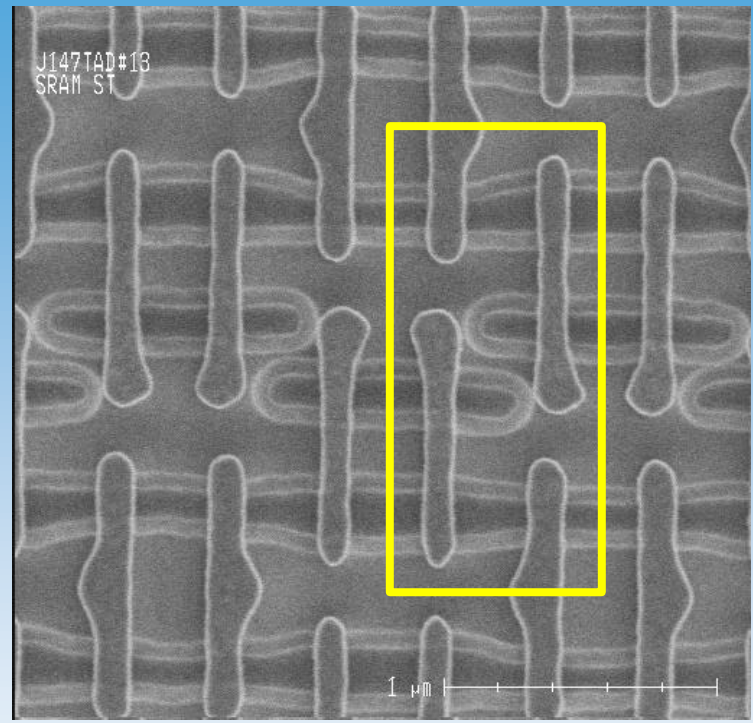
Status

- 90 nm design rules already validated on fully functional test chips
- Proven 1 Mbit and 4 Mbit of embedded static RAM (SRAM)
- Prototyping (300mm) as per end 2002
- Multi-purpose Wafer (MPW) service (200mm) as per today
- Initial SRAM density of 735 kbit/mm^2, fully compliant with design rules



1.36 µm^2 SRAM memory array top view at gate level

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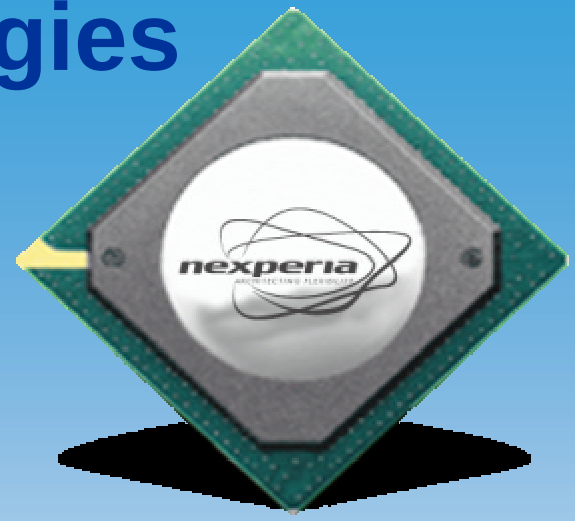
Differentiating technologies



These CMOS technologies are the fuel of our System-on-a-Chip strategy

- High density, high performance and low power
- Embedded memory (incl. Flash)

Complemented by

- Nexperia architectures
  - Delivering flexibility
  - Reducing time-to-market
- Efficient IP based design (Sea of IP)
  - Reuse of hardware and software (CoReUse / MoReUse)
  - HDLi for IP generation and delivery
- Rapid Silicon prototyping for first-time right design

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- **Trend of Collaboration and Alignment**
- **Philips, ST and TSMC Joint Development Project**
- **Standardized Design Rules**
- **JDP and ITRS Roadmap**
- **TSMC Capacity Plan**

Trend of Collaboration and Alignment

- Clear trend toward alignment, collaboration and joint development of advanced semiconductor technology
- Driven by System-on-Chip (SoC) requirement of effective IP development and sharing
- Also driven by needs of foundry capacity as alternative wafer sources
- Accelerated by R&D costs and time-to-volume pressures
- Differentiation sustained by uniqueness of individual designs, including novel use of specialized process modules such as analog, RF and bipolar elements

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Philips, ST and TSMC Joint Development

- Synergistic project involving leaders in advanced technology, product development, and wafer manufacturing
- ST and Philips are among world leaders in advanced technology and product development with both depth and breadth, well-positioned to win in SoC marketplace
- TSMC contributes its experience in advanced technology and ability to ramp production facilities in large volumes with robust IP, library and design service support

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Standardized Design Rules

- Years of experience with 500+ customers in variety of application areas have provided
  - Deep understanding of design parameter requirement
  - Unique position to translate these to efficient manufacturing
- Enables us to define common set of design rules for advanced process technology, encompassing:
  - Widest possible variety of applications
  - Aggressive transistor performance
  - Industry-leading layout density
  - Highest quality and yields
  - Competitive manufacturing costs

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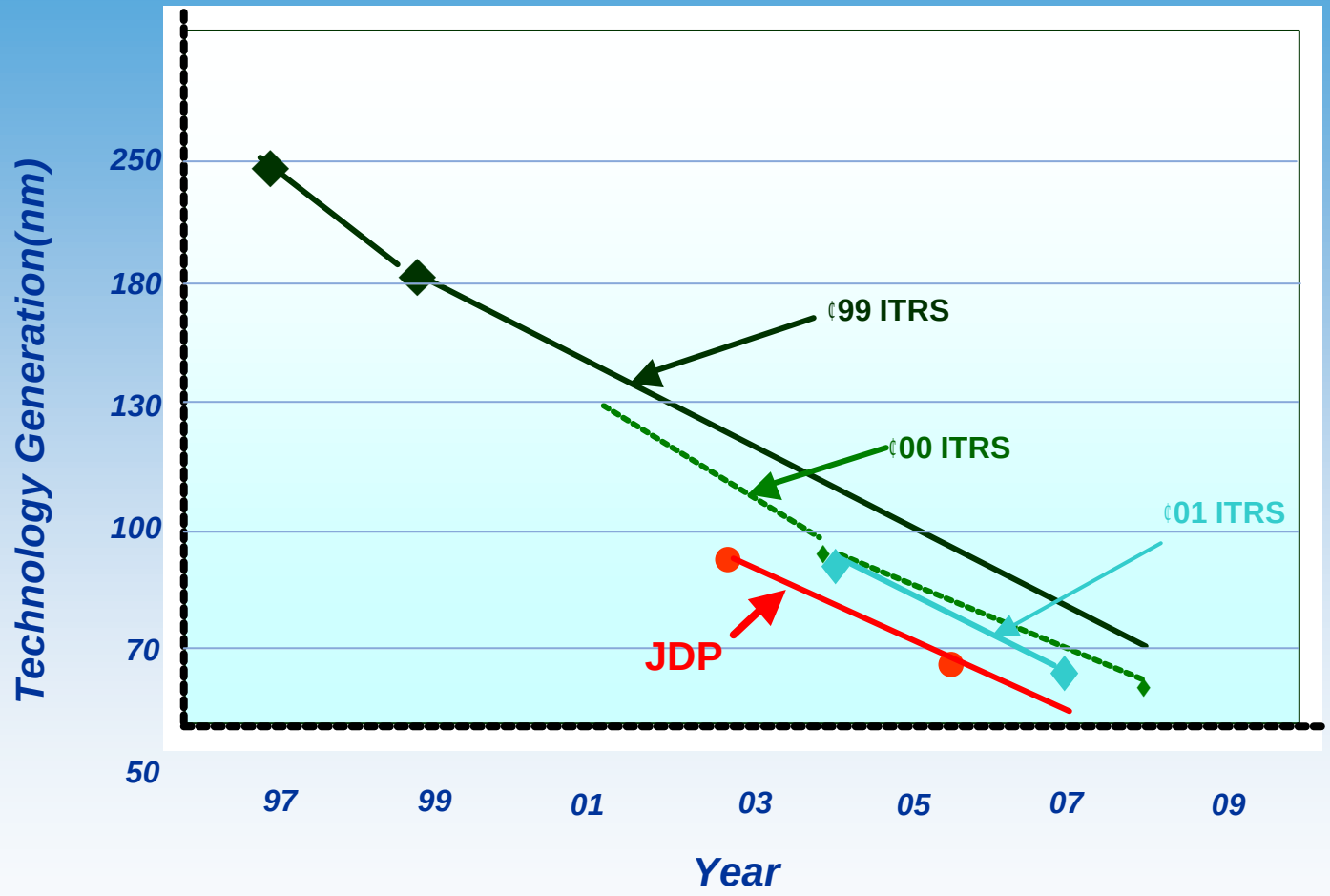
JDP Roadmap Leads ITRS



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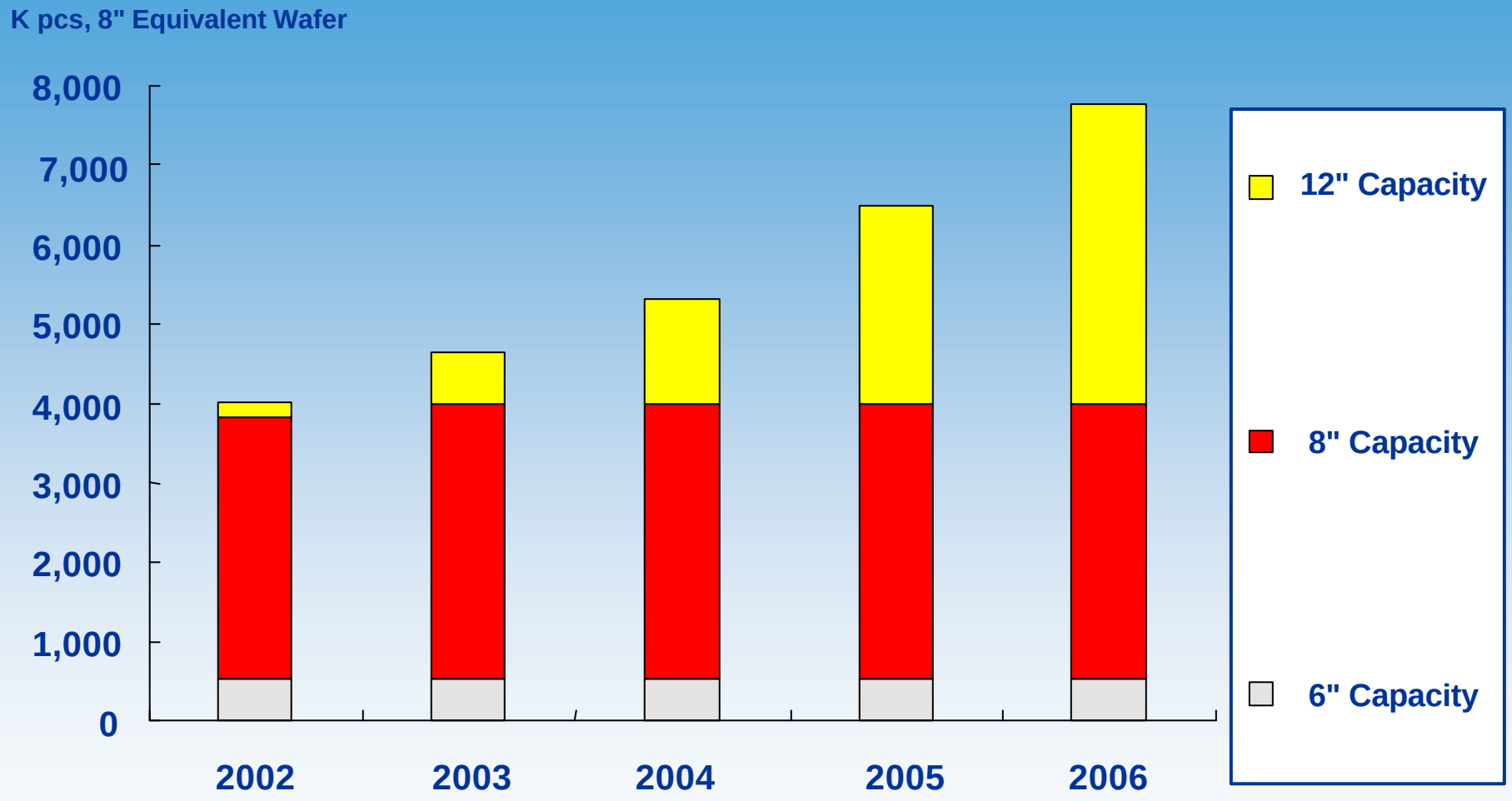
5-Year Installed Capacity Plan



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